PATENT ABSTRACTS OF JAPAN

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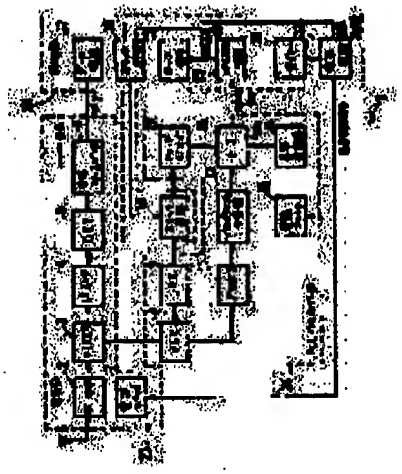
(71)Applicant : SHARP CORP
(72)Inventor : SUMIKAWA KEIICHIRO

(54) PHASE LOCKED LOOP CIRCUIT

(57)Abstract:
PURPOSE: To reduce the lock time at intermittent operation by providing a switching means and a voltage storage means storing an input v ltage to a voltage controlled oscillator circuit just before the open circuit between a phase comparator and an LPF.
CONSTITUTION: The switching circuit 16 interposed between the phase comparator (PD) 13 and the LPF 9, a charge pump 10 storing an input voltage to the voltage controlled oscillator circuit (VCO) 8 just before the op n circuit and a switch control means 18 opening a loop by the switch 16 in the presence of the open circuit command, giving the said storage voltage to the VCO 8 when the open command exists and closing the loop by the switch 16 when the phase difference detected by the PD 13 reaches a prescribed value or below, are provided. When the power of the PLL circuit is switched from OFF to ON in the intermittent peration, the preceding frequency is taken over. Moreover, the loop is closed with a large phase difference and the frequency is not largely deviated. The lock time at the intermittent operation is shortened by the operation.



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審査請求　未請求　発明の数 1　(全5頁)

⑭発明の名称　フェーズ・ロックド・ループ回路

⑳特願　昭62-195460
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㉑発明者　香川　恵一郎　大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内
㉑出願人　シャープ株式会社　大阪府大阪市阿倍野区長池町22番22号
㉔代理人　弁理士　本庄　武男

明細書

1．発明の名称

フェーズ・ロックド・ループ回路

2．特許請求の範囲

1．位相比較回路と、ローパスフィルタと、電圧制御発振回路とがループを形成してなるフェーズ・ロックド・ループ回路において、

位相比較回路とローパスフィルタの間またはローパスフィルタと電圧制御発振器の間に介設されてループをオープンする手段と、オープン信号の電圧制御発振回路への入力電圧を設定する電圧設定手段と、オープン指令があると前記スイッチ手段でループをオープンすると共にクローズ指令があると前記設定電圧を前記電圧制御発振回路に入力し前記位相比較回路で位相差を検出し位相差が所定値以下となったときに前記スイッチ手段でループをクローズするスイッチ制御手段とを具備したことを特徴とするフェーズ・ロックド・ループ回路。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は、フェーズ・ロックド・ループ回路に関し、更に詳しくは、間欠動作させる場合に周波数引き込み範囲を狭くできるようにしたフェーズ・ロックド・ループ回路に関する。

〔従来の技術〕

コードレス電話やページャ等の携帯用無線機においては、電池の消耗を防ぐために、受信すべき電波の有無がある程度では間欠動作を行わせている。

即ち、受信部等全体に電力を供給して電波を受信できる状態で待機する時と受け動作と、必要最低限の部分以外は電力の供給をカットして電波を受信できないが電力消費を節約する休止動作とを交互に繰り返すことを行なっている。

フェーズ・ロックド・ループ回路（以下、PLL回路という）は、携帯用無線機のチューナ部のシンセサイザーとして広く使用されており、上記間欠動作時には、PLL回路も間欠動作させられている。

（発明が解決しようとする問題点）

チューナ部にPLL回路を用いた場合、PLL回路の周波数引き込み範囲（プルインレンジ）を経てロックされるまでの時間（ロックタイム）は正しい受信状態に入れない。従って、ロックタイムは短い方が好ましい。

ところが、PLL回路を間欠動作させると、その都度電源オフから立ち上がるため、前記ロックタイムが長くなってしまう問題点がある。

従って、本発明の目的とするところは、間欠動作時におけるロックタイムを短縮可能としたPLL回路を提供することにある。

（問題点を解決するための手段）

本発明のPLL回路は、位相比較回路と、ローパスフィルタと、電圧制御発振回路とがループを形成して成るフェーズ・ロックド・ループ回路において、位相比較回路とローパスフィルタの間またはローパスフィルタと電圧制御発振回路の間に介設されてループをオープンする手段と、オープン直前の電圧制御発振回路への入力電圧を記憶する記憶手段と、オープン指令があると前記スイッチ手段でループをオープンすると共に、クローズ指令があると前記記憶電圧を前記電圧制御発振回路に入力し前記位相比較回路で位相差を検出し位相差が所定値以下となったときに前記スイッチ手段でループをクローズするスイッチ制御手段とを具備したことを構成上の特徴とするものである。

〔作用〕

本発明のPLL回路では、電圧記憶手段によって電圧制御発振回路への入力電圧を記憶しておくことが出来るので、間欠動作時において、PLL回路の電源がオフからオンに切り替わった時、以前の周波数からスタートできる。従って、初期の周波数ずれを少なく出来る。

また、スイッチ制御手段によって、位相差が所定量以下となった時にループをクローズすることが出来るので、位相差が大きいままループをクローズにして、周波数を大きく外してしまうことが防止される。

そこで、これらの作用より、間欠動作時におけるロックタイムを短縮することが出来る。

そして、携帯用無線機等で間欠動作させる時の待ち受け時間をロックタイムの短縮に伴って短縮することが出来るようになるから、消費電力を一層低減できるようになる。

（実施例）

以下、図に示す実施例に基づいて本発明を更に詳しく説明する。ここに第1図は本発明の一実施例のPLL回路を含む携帯用受信機のブロック図、第2図は本発明におけるスイッチ手段と電圧記憶手段とに対応する回路部分の具体的例示図、第3図は本発明におけるスイッチ制御手段に対応する回路部分の具体的例示図、第4図は第1図に示す各部の信号波形図である。尚、図に示す実施例により本発明が限定されるものではない。

第1図に示す携帯用受信機1は、受信部23と、PLLシンセサイザー部24と、制御部25の3つの部分からなっている。

受信部23は、従来公知の構成と同様であり、間欠動作のための電源スイッチ回路7が設けられている。

PLLシンセサイザー部24は、電圧制御発振回路8と、ローパスフィルタ9と、チャージポンプ10と、プリスケーラ11と、プログラマブル分周器12と、位相比較回路13と、基準発振回路14とを有し、また、間欠動作のための電源スイッチ回路15を有している。

ここで注意すべきことは、ローパスフィルタ9とチャージポンプ10との間に、スイッチ回路18が介設されていることである。

位相比較回路13は、チャージポンプ10への出力の他に、位相差のあるときにパルスが出現するアンロック信号を出力している。

第2図は、ローパスフィルタ9、スイッチ回路18、チャージポンプ10を具体的に例示したものである。

制御部25は、前記スイッチ回路18を制御するためのスイッチ制御回路19と、間欠動作を制御するためのタイマー回路21および電源制御回路22と、前記位相比較回路13からのアンロッ

9信号に応じて位相比較器信号を出力するパルス幅検出回路２０とを具備している。位相差信号は、前記スイッチ制御回路１９に入力されている。

第３図は、スイッチ制御回路１９，パルス幅検出回路２０を具体的に例示したものである。

次に、第１図～第３図及び第４図に示す信号波形図を参照し、順次動作の作動を説明する。

まず、待ち受け動作の状態では、受信部２３，アレシンセサイザー部２４，制御部１５の全てに電力が供給され、電波を受信できる状態で待機している。ここで前記周波数は１波、通話用の複数の通話チャンネルと、着信制御用の制御チャンネルとを有しているが、待ち受け動作では、前記チャンネルの１波を待っている。

待ち受け動作を所定時間継続すると、タイマー回路２１及び電源制御回路２２から出力される電源オン信号が「L」になる。すると、第５図に示すようにスイッチ回路１９がオフされ、第２図に示すようにローパスフィルタ９のコンデンサC８は信号の電圧を保持した状態となる。

する周波数ふらつき、それは他の待ち受け動作における周波数とほぼ等しい周波数である。従って、立ち上がりに要する時間が短縮される。

ところで、位相比較回路１８に入力される電圧制御発振回路９側からの信号と基準発振器１４からの信号の位相差が大きいと、同符号の周波数が合致していても、ループがクローズされた時に周波数が大きく外れてしまう恐れがある。

しかし、スイッチ回路１９は、位相差検出信号を待ってから閉じられるため、かかる周波数のずれは防止される。即ち、第３図に示すＩＮＨＴ期間によって、電源立ち上がり時にはスイッチ回路１９を閉じないようにする。そして、位相差が大きい時に出力されるアンロック信号が入力されている間は、スイッチ回路１１を閉じないようにする。そして、電源が完全に立ち上がり、且つ、位相差が小さくなってアンロック信号が入力されない時にスイッチ回路１６が閉じられる。

そこで結局、周波数がほぼ合致し、且つ、位相差のない状態でループがクローズされるので、周

電源　部　２２は、スイッチ回路１９をオフにした後、電源スイッチ回路７及び１５を作動し、受信部２３とアレシンセサイザー部２４の電源を遮断する。また、制御部２５のデータ設定回路１７，ロック検出回路１８，パルス幅検出回路２０の電源を遮断する。かくして、電源の無駄な出力ないか、消費電力を節制した休止動作に移行する。

休止動作を所定時間継続すると、タイマー回路２１及び電源制御回路２２は、電源オン信号を「H」にし、受信部２３及びアレシンセサイザー部２４の電源をオンとする。また、制御部２５のデータ設定回路１７，ロック検出回路１８，パルス幅検出回路２０の電源をオンにする。

しかし、スイッチ回路１９は、電源オン信号が「H」となっても、パルス幅検出回路２０からの位相差信号が入力されないかぎり、ループをクローズにしない。

そこで、電圧制御発振器９の出力の周波数は、ローパスフィルタ８に保持されていた電圧に対応

数ばかりを生じず、短時間でアレシ回路はロックする。

かくして、アレシ回路のロックタイムを短縮できるため、待ち受け動作の時間を短縮できるようになる。そこで、送信すべき電波の受信があるまでの時間に通常周波信号１が消費する電力を低減できることとなる。

【発明の効果】

本発明によれば、位相比較器と、ローパスフィルタと、電圧制御発振器とループを形成してなるフェーズ・ロックド・ループ回路において、位相比較器とローパスフィルタの間または、ローパスフィルタと電圧制御発振器の間に介装されてループをオープンする手段と、オープン直前の電圧制御発振器への入力電圧を記憶する電圧記憶手段と、オープン指令があると自動スイッチ手段でループをオープンするとともにクローズ指令があると前記記憶電圧を前記電圧制御発振器に入力し、前記位相比較器で位相差を検出し位相差が所定値以下となったときに前記スイッチ手段でループ

をクローズするスイッチ制御手段とを具備したことを特徴とするフェーズ・ロックド・ループ回路が提供され、これにより周波数引き込みに要する時間すなわちロックタイムを短縮できるようになる。

そこで、かかるフェーズ・ロックド・ループ回路を用いた携帯用受信機において、間欠動作をする時の立ち上がり動作の時間を短縮できることとなり、低消費電力化を促進できる。

4. 図面の簡単な説明

第1図は本発明の一実施例のPLL回路を含む携帯用受信機のブロック図、第2図は本発明におけるスイッチ手段と電圧保持手段とに対応する回路部分の具体的構成図、第3図は本発明におけるスイッチ制御手段に対応する回路部分の具体的構成例示図、第4図は第1図に示す回路図の各部の信号波形図である。

〔符号の説明〕

1…携帯用受信機

8…電圧制御発振回路

9…ローパスフィルタ

10…チャージポンプ

12…位相比較回路

15…スイッチ回路

19…スイッチ制御回路

20…パルス幅検出回路

21…タイマー回路

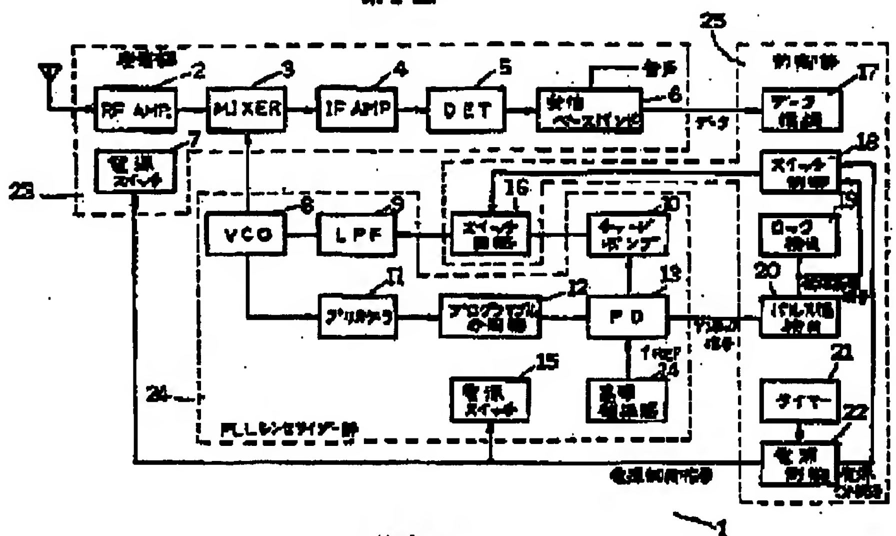
22…電源制御回路

7，13…電源スイッチ回路。

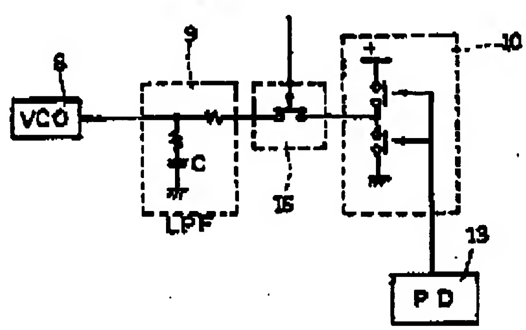
出願人　シャープ株式会社

代理人　弁理士　青山　葆

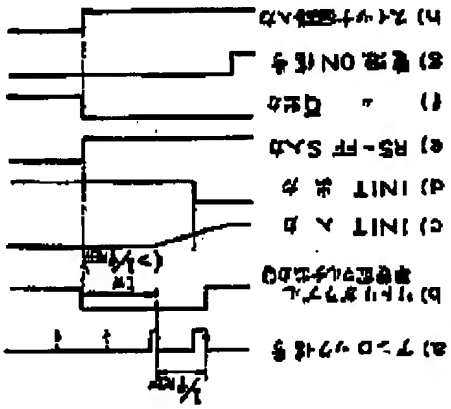
第1図



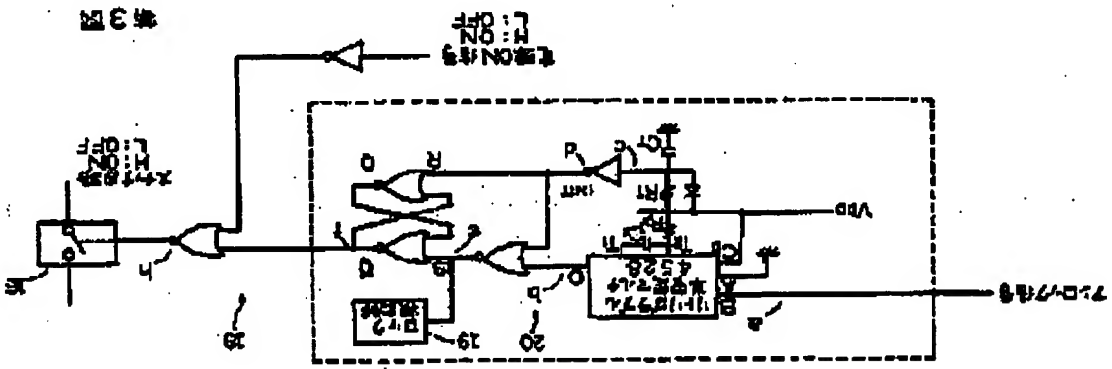
第2図



第4図



第3図



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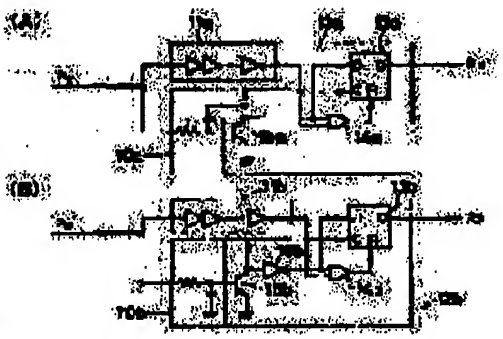
(21)Application number : 05-207102
(22)Date of filing : 28.07.1993

(71)Applicant : NEC CORP
(72)Inventor : JOKURA ATSUSHI

(54) PLL CIRCUIT

(57)Abstract:
PURPOSE: To improve S/N of the PLL circuit in the frequency synthesizer of a reception system by providing a dead zone for phase comparison and realizing stable synchronous convergence.
CONSTITUTION: A phase leading PD pulse is delayed by a delay device 11b and is inputted to the clock input of a D-FF 13b. The PD pulse is integrated by a time constant circuit 10b, and this integral waveform is compared with the threshold of a transistor TR 15b, and, a pulse is generated when it is larger than this threshold. This pulse is inputted to the data input of the D-FF 13b to latch the PD pulse, and the D-FF 13b is res t by an OR gate 14b at the time of disappearance of the PD pulse. Its Q output RD is supplied to a charge pump and a loop filter to obtain the control voltage of a VCO. Consequently, the dead zone is determined by CR of the time constant circuit 10b and the threshold of the TR 15b, and the PD pulse larger than the dead zone is outputted as it is, and therefore, synchronous convergence is stabilized.



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[Pat nt number]	2655043
[Date of registration]	30.05.1997
[Numb r of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] An armature-voltage control oscillation means and a phase-comparison means to make the phase comparison of this oscillation output frequency signal and external oscillation signalling frequency, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, The PLL circuit characterized by being constituted including a latch means to cancel this latch state when the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means so that the aforementioned control voltage may be generated using this latch output.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.
[0002]
[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.
[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.
[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.
[0005] Drawing 5 is the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A. reference frequency signal fR with which the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed [21] to the clocked-into terminal of 1st D-FF22 for a charge pump and 22 The 1st delayed delay circuit and dividing signal fP with which 25 was impressed to the clocked-into terminal of 2nd D-FF23 It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.
[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.
[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.
[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.
[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.
[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).
[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.
[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ=

"0" is chosen. It is f R first. fP When the phase is in agreement, it is t... is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.
[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.
[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contrast is an output Q1 within in 10ns. Vt Output PD corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same -- fP if it comes out 10 or less ns when it becomes earlier than fR -- output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.
[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.
[0016]
[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.
[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7 . In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.
[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.
[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.
[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.
[0021]
[Means for Solving the Problem] A phase-comparison means to make the phase comparison of an armature-voltage control oscillation means, and this oscillation output frequency signal and external oscillation signalling frequency according to this invention, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.
[0022]
[Example] It explains in detail, referring to a drawing about the example of this invention below.
[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2 . They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.
[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.
[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.
[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1 . First, if

drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a.
[0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.
[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.
[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.
[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.
[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timin timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.
[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.
[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.
[0035] phase-lead-lag-network signal PD exceeding a dead zone ******** -- without the wave of the pulse changing, since there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained.
[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone tM. It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.
[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.
[0038]
[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.
[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

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PRIOR ART

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.
[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.
[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.
[0005] For a charge pump and 22, 21 is the reference frequency signal fR with which drawing 5 was the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A, the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed to the clocked-into terminal of 1st D-FF22. 25 is the 1st delayed delay circuit and the dividing signal fP impressed to the clocked-into terminal of 2nd D-FF23. It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.
[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.
[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.
[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.
[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.
[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).
[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.
[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ= "0" is chosen. It is f R first. fP When the phase is in agreement, it is the output R1 of a delay circuit. R2 What is generated is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.
[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contr corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same – fP if it comes out 10 or less ns when it becomes earlier than fR – output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.

[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.

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EFFECT OF THE INVENTION

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.
[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.
[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7 . In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.
[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.
[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.
[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

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MEANS

[Means for Solving the Problem] They are the time constant circuit which is the PLL circuit which includes an armature-voltage-control oscillation means, a phase-comparison means make the phase comparison of this oscillation output-frequency signal and external oscillation signalling frequency, and a control-voltage generation means generate the control voltage of the aforementioned armature-voltage-control oscillation means according to this phase-comparison output according to this invention, and the aforementioned control-voltage generation means carries out as an input in a delay means to by_which the aforementioned phase-comparison output is delayed, and the aforementioned phase-comparison output, and the output of the aforementioned delay means. When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

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EXAMPLE

[Example] It explains in detail, referring to a drawing about the example of this invention below.
[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2 . They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.
[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.
[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.
[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1 . First, if drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into delay circuit 11a and time constant circuit 10a, respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a.
[0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.
[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.
[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.
[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.
[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timin timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.
[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.
[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.

[0035] phase-lead-lag-network signal PD exceeding a dead zone there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained

[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone tM. It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.

[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the PLL circuit by this invention.
[Drawing 2] It is the circuit diagram showing an example of the filter circuits 4a and 4b of drawing 1 .
[Drawing 3] It is each part operation wave form chart of the circuit of drawing 2 .
[Drawing 4] It is the phase-comparison property view of the PLL circuit by this invention.
[Drawing 5] It is the circuit diagram of the phase comparator of the conventional PLL circuit.
[Drawing 6] It is each wave form chart of the circuit of drawing 5 of operation.
[Drawing 7] It is each wave form chart of the circuit of drawing 5 of operation.
[Drawing 8] It is the phase-comparison property view of the circuit of drawing 5 .
[Description of Notations]
1 Reference Frequency VCO
2 Counting-down Circuit
3 Phase Comparator
4a, 4b Filter circuit
5 Charge Pump
6 Loop Filter
7 VCO
10a, 10b Time constant circuit
11a, 11b Delay circuit
12a, 12b Latch circuit
13a,13b D-FF
14a, 14b OR gate
15a, 15b Transistor
16b Inverter

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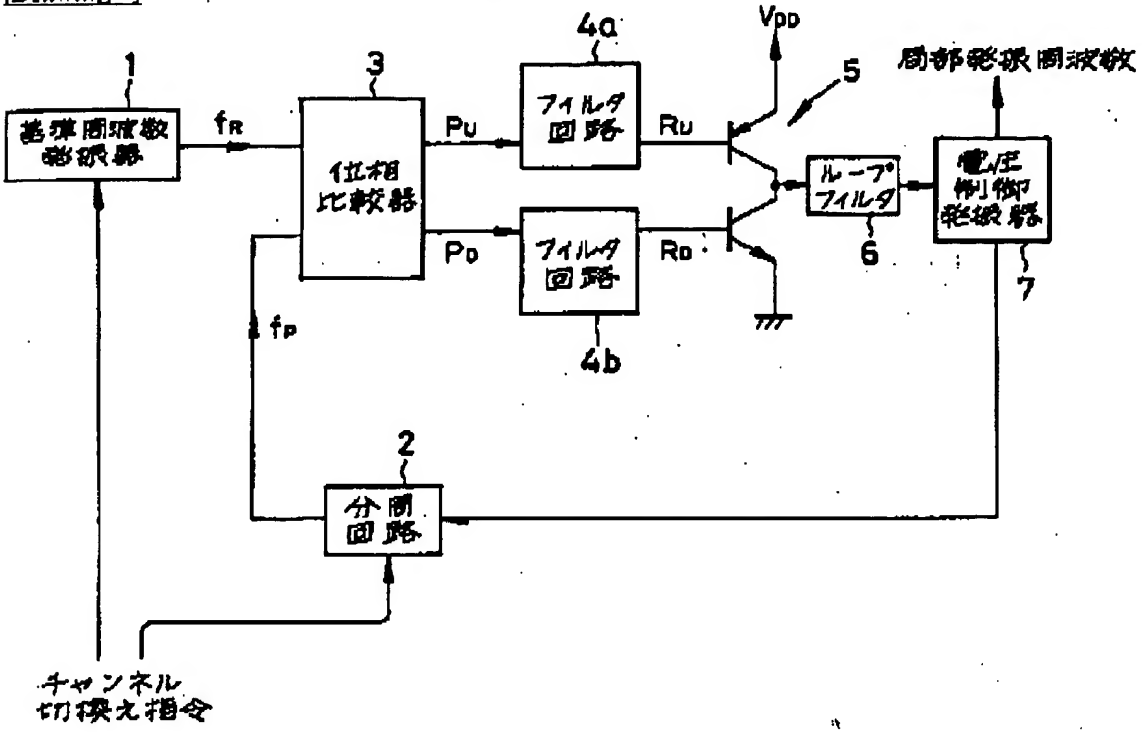
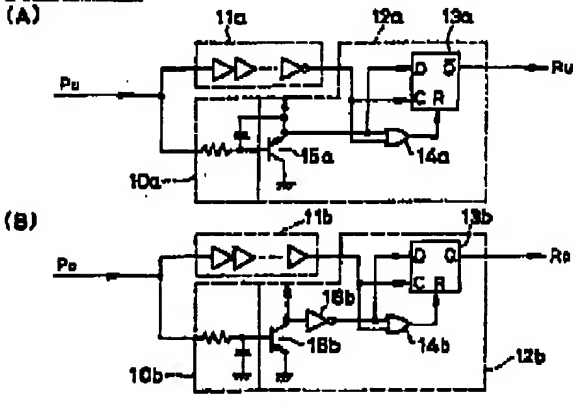
DRAWINGS

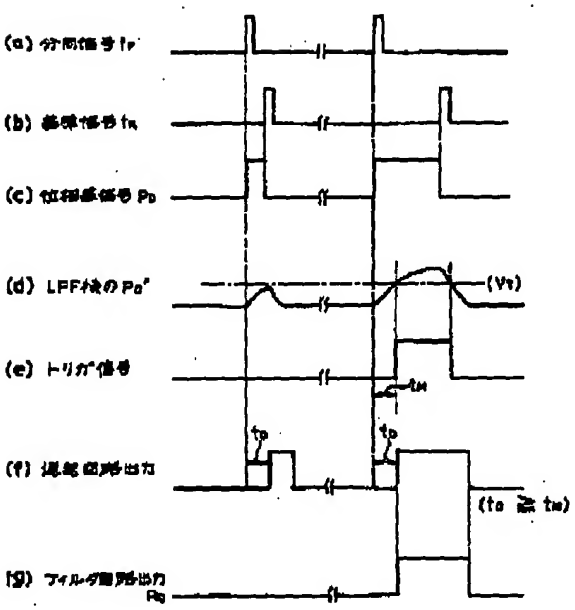
[Drawing 1]



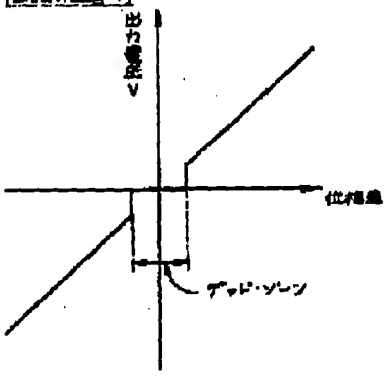
[Drawing 2]



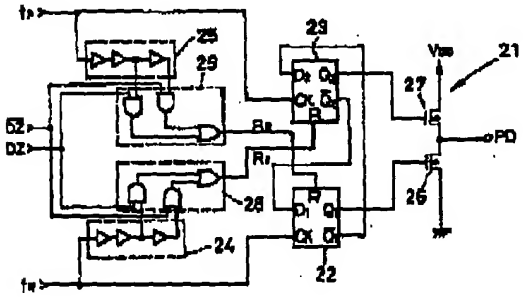
[Drawing 3]



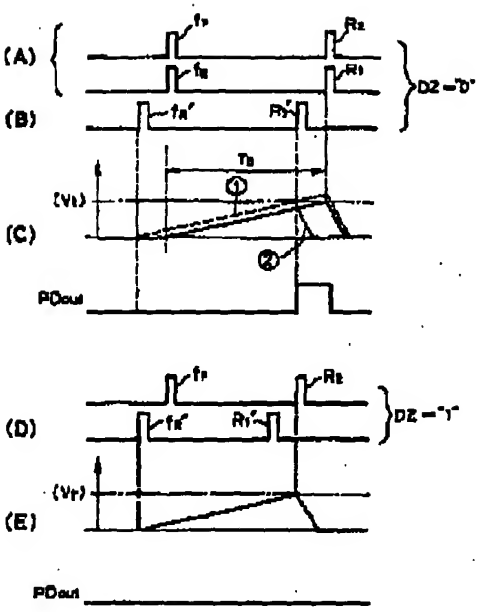
[Drawing 4]



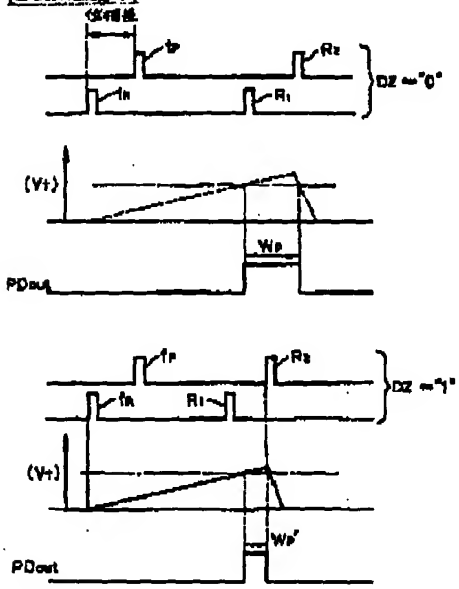
[Drawing 5]



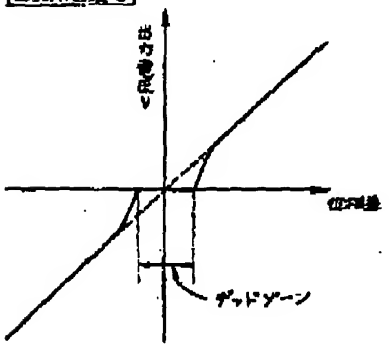
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]